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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,476	01/27/2004	Koji Shimizu	118245	9140

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EXAMINER	
AMADIZ, RODNEY	
ART UNIT	**PAPER NUMBER**
2629	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/764,476	SHIMIZU ET AL.	
	Examiner	Art Unit	
	RODNEY AMADIZ	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9 and 11-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9 and 11-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

076446

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 20, 2009 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 9 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al. (U.S. Patent 7,057,589—hereinafter "Shin") in view of Kuwabara et al. (U.S. Patent—hereinafter "Kuwabara") in view of Watanabe et al. (U.S. Patent 5,534,809—hereinafter "Watanabe").

As to **Claim 9**, Shin teaches an electro-optical device comprising:

a substrate having one or more edges each at a peripheral portion of the substrate ***(Fig. 4, 210)***;

scanning lines ***(Fig. 4, X1-XM)***;

data lines ***(D1-Dn and Y1-Y3n)***;

pixels arranged over the substrate at positions that correspond to intersections between the scanning lines and the data lines, the pixels forming a matrix ***(Fig. 4, 210 and 212)***;

selection-signal input terminals arranged close together ***(Fig. 5, at the far left, note the three nodes at the intersections of lines 241, 243 and 245 with the lines going into MR1, MG1 and MB1, respectively)***, each of the selection-signal input terminals being supplied with a selection signal ***(Fig. 5, HR, HG and HB)***;

image-signal input terminals supplied with image-signals ***(Fig. 5, D1)***,

a selecting circuit ***(Fig. 4, 240)*** selectively supplying image signals to the data lines on the basis of the selection signals ***(See Fig. 5, wherein data signal D1 is supplied to Y1, Y2 and Y3 on the basis of the selection signals (241, 243 and 245) and Col. 7, lines 9-41)***, and the selecting circuit including switching elements ***(Fig. 5, MR1, MG1 and MB1)*** having first input-output terminals connected to the data lines ***(Fig. 5, note connection to Y1, Y2 and Y3)***, a second input-output terminal connected to a node supplying the image signals ***(Fig. 5, note connection to D1 through node)***, and control input terminals to which the selection signals are supplied ***(Fig. 5, note connections from 241, 243 and 245 to MR1, MG1 and MB1, respectively)***;

a selection-signal supplying device to supply the selection signals to the selection-signal input terminals ***(Fig. 5, note signals HR, HG and HB coming from controller (not shown)—Col. 7, lines 9-41)***, and

selection-signals supplying lines that connect the selection-signal input terminals to the control input terminals; ***(Fig. 5, note the signal lines that extend downward and then left from lines 241, 243 and 245)***;

the control input terminals of the selection circuits being arranged in the same direction as that of the selection-signal input terminals and in the same order as the corresponding selection-signal input terminals ***(See Fig. 5)***.

Shin fails to teach the arrangement wherein the selection-signal input terminals and the image-signal input terminals are aligned along the same edge of the substrate and located between the matrix and the corresponding edge. Examiner cites Kuwabara to teach that it is well known to align signal input terminals along an edge of a substrate ***(See Figs. 1, 5, 7, 9a, 10, 11, 12 and 17—left edge)*** between the matrix and the corresponding edge ***(See Figs. 1, 5, 7, 9a, 10, 11, 12 and 17)***. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to incorporate the teachings of Kuwabara (that is, placing the input terminals of the signal lines along the same edge and between the matrix) in the electro-optical device taught by Shin in order to keep all connections at one end, thereby making cleaner connections on the substrate.

Shin, as modified by Kuwabara, fails to teach all of the signal-supplying lines having the same length from the corresponding selection-signal input terminal to the control input terminal of the corresponding switching element to compose an equivalent low-pass filter. Examiner cites Watanabe to teach that the concept of having wiring lines of the same length is well known ***(Col. 6, lines 45-48)***. At the time the invention

was made it would have been obvious to a person of ordinary skill in the art to incorporate the teachings of Watanabe (i.e. make wiring lines with the same length) in the electro-optical device taught by Shin as modified by Kuwabara so that each signal-supplying line, from the selection-signal input terminal to the control input terminal, may be equal in load capacitance ***(Col. 6, lines 45-48)***. The resulting combination of Shin, Kuwabara and Watanabe yields an equivalent low-pass filter.

As to **Claim 11**, Shin, teaches an electronic apparatus comprising the electro-optical device of Claim 9 ***(Shin—See Fig. 4)***.

As to **Claim 12**, Shin teaches that each of the selection-signal supplying lines includes a first wiring line extending from the selection-signal input terminal in a same direction as the direction as the direction in which the data lines extend, and extends in a direction intersecting the direction in which the data lines extend ***(Fig. 5, (left side) note the intersection of lines 241, 243 and 245 with the first wiring lines that extend downwards in the direction of the data lines and then to the right (in a direction intersecting the direction of the data lines) towards MR1, MG1 and MB1, respectively)***.

Shin fails to teach a second wiring line extending from the first wiring line to the control input terminal in a same direction as the direction in which the data lines extend. However, the specification shows no apparent benefits from having a second wiring line extend from the first wiring line to the control input in a same direction as the direction in which the data lines extend. Therefore, having a second wiring line extend in specific directions is clearly a design choice based on the specific requirement of the claim.

Furthermore, it would have been obvious to a person of ordinary skill in the art to add a second wiring line to the electro-optical device taught by Shin and extend it in any direction since extending the wiring lines in any direction would perform equally well at carrying and providing the intended signal.

As to **Claim 13**, Shin, as modified by Kuwabara, fails to teach that all second wiring lines, that extend from a respective control input terminals to a same first wiring line, have the same width. Examiner cites Watanabe to teach that the concept of having wiring lines of the same width is well known ***(Col. 6, lines 45-48)***. At the time the invention was made it would have been obvious to a person of ordinary skill in the art to incorporate the teachings of Watanabe (i.e. make wiring lines with the same width) in the electro-optical device taught by Shin as modified by Kuwabara so that each second wiring line, may be equal in load capacitance ***(Col. 6, lines 45-48)***. The resulting combination of Shin, Kuwabara and Watanabe yields an equivalent low-pass filter.

4. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin, Kuwabara and Watanabe as applied to claims 9 and 11-13 above, and further in view of Haga et al. (USPGPUB 2003/0067434—hereinafter "Haga").

As to **Claim 14**, Shin, as modified by Kuwabara and Watanabe, fails to teach secondary selection-signal input terminals arranged close together, the secondary selection-signal terminals being located between the matrix and the corresponding edge of the substrate and being aligned with the selection-signal input terminals and the

image-signal input terminals along the corresponding edge, each first wiring line, that extends from a respective selection-signal input terminal, extending to a respective secondary selection-signal input terminal. Examiner cites Haga to teach a second input terminal provided as the second end of the signal-supplying lines, wherein each first wiring line that extends from a respective selection-signal input terminal, extends to a respective secondary selection-signal input terminal. ***(Fig. 20, Reference Number 107 and note that 108 is being fed to both ends of 107—See also Pg. 5, ¶ 80, Pg. 7, ¶ 117 and Pg. 13, ¶ 218)***. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to incorporate a second input terminal to the signal supplying line as taught by Haga in the electro-optical device taught by Shin, as modified by Kuwabara and Watanabe, in order to reduce signal delay on the wiring lines. Furthermore, the combination of Shin and Kuwabara already teaches that the selection-signal terminals are located between the matrix and the corresponding edge of the substrate and Haga teaches that the secondary input terminals are aligned with the first selection-signal input terminals; therefore, the combination of Shin, Kuwabara, Watanabe and Haga meet the claim limitations.

As to **Claim 15**, Shin teaches that each of the selection-signal supplying lines includes a first wiring line extending from the selection-signal input terminal in a same direction as the direction as the direction in which the data lines extend, and extends in a direction intersecting the direction in which the data lines extend ***(Fig. 5, (left side) note the intersection of lines 241, 243 and 245 with the first wiring lines that extend downwards in the direction of the data lines and then to the right (in a***

direction intersecting the direction of the data lines) towards MR1, MG1 and MB1, respectively).

Shin fails to teach a second wiring line extending from the first wiring line to the control input terminal in a same direction as the direction in which the data lines extend. However, the specification shows no apparent benefits from having a second wiring line extend from the first wiring line to the control input in a same direction as the direction in which the data lines extend. Therefore, having a second wiring line extend in specific directions is clearly a design choice based on the specific requirement of the claim. Furthermore, it would have been obvious to a person of ordinary skill in the art to add a second wiring line to the electro-optical device taught by Shin and extend it in any direction since extending the wiring lines in any direction would perform equally well at carrying and providing the intended signal.

As to **Claim 16**, Shin, as modified by Kuwabara and Haga, fails to teach that all second wiring lines, that extend from a respective control input terminals to a same first wiring line, have the same width. Examiner cites Watanabe to teach that the concept of having wiring lines of the same width is well known ***(Col. 6, lines 45-48)***. At the time the invention was made it would have been obvious to a person of ordinary skill in the art to incorporate the teachings of Watanabe (i.e. make wiring lines with the same width) in the electro-optical device taught by Shin, as modified by Kuwabara and Haga, so that each second wiring line, may be equal in load capacitance ***(Col. 6, lines 45-48)***. The resulting combination of Shin, Kuwabara, Haga and Watanabe yields an equivalent low-pass filter.

Response to Arguments

5. Applicant's arguments with respect to claims 9 and 11-16 have been considered but are moot in view of the new ground(s) of rejection.

Inquiries

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RODNEY AMADIZ whose telephone number is (571)272-7762. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/R. A./
Examiner, Art Unit 2629
5/15/09